Docket No.: 055123.P086R

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Gregory L. Schaffer	Examiner:
Reissue Application No.:	Art Group:
Filed:	
For: Dual Interleaved DC to DC Switching Circuits Realized in an Integrated Circuit	
Reissue of: USP 5,870,296	
Issued: February 9, 1999	

AMENDMENT UNDER 37 C.F.R. § 1.173(b)

BOX REISSUE
Assistant Commissioner for Patents
Washington, DC 20231-9998

Sir:

In accordance with 37 C.F.R. § 1.173(b), Applicant respectfully submits that the proposed amendments be incorporated into the above-identified Reissue application prepared in compliance with 37 C.F.R. § 1.173(a) and enclosed herewith. The proposed amendments are set forth below:

22. A DC to DC switching circuit for controlling power switching devices in a DC to DC converter having a plurality

of interleaved converter circuits operating into a common load, comprising:

a plurality of pulse width modulators each controlling power switching devices of one of the plurality of interleaved converter circuits;

a feedback circuit responsive to a voltage across the common load;

control circuits for controlling the plurality of pulse width modulators responsive to the feedback circuit and a commanded output voltage, and for adjusting a nominal duty cycle of the plurality of interleaved converter circuits;

the plurality of pulse width modulators and the control circuits being in a single integrated circuit.

23. The DC to DC switching circuit of claim 22 further comprising a current sense circuit for balancing current in the plurality of interleaved converter circuits.

24. The DC to DC switching circuit of claim 22 further comprised of an integrator having an output responsive to the integral of an error signal, the error signal being responsive to the voltage across the common load and a desired voltage, the control circuits also being responsive to the output of integrator.

25. The DC to DC switching circuit of claim 24 wherein a time constant of the integrator is adjustable by the

selection of at least one component external to the integrated circuit.

26. The DC to DC switching circuit of claim 24 further comprised of a differentiator having an output responsive to the rate of change of the voltage across the common load, the control circuits also being responsive to the output of differentiator.

27. The DC to DC switching circuit of claim 26 wherein the time constant of the differentiator is adjustable by the selection of at least one component external to the integrated circuit.

28. The DC to DC switching circuit of claim 22 wherein the control circuits are also responsive to rapid decreases in the voltage across the common load to turn on the plurality of converter circuits independent of the phase of the plurality of pulse width modulators.

29. The DC to DC switching circuit of claim 28 wherein the control circuits are also responsive to rapid increases in the voltage across the common load to turn off the plurality of converter circuits independent of the phase of the plurality of pulse width modulators.

30. The DC to DC switching circuit of claim 22, wherein the plurality of pulse width modulators consist of a pair of pulse width modulators.

31. The DC to DC switching circuit of claim 22 wherein the feedback circuit is in the single integrated circuit.

32. A DC to DC switching circuit for controlling power switching devices in a DC to DC converter having a plurality of interleaved converter circuits operating into a common load, comprising:

a plurality of pulse width modulators each controlling power switching devices of one of the plurality of interleaved converter circuits;

a feedback circuit responsive to a voltage across the common load;

control circuits being responsive to the feedback circuit and a commanded output voltage to control a nominal duty cycle of the plurality of converter circuits, the control circuits also adjusting a relative duty of the plurality of converter circuits;

the plurality of pulse width modulators and the control circuits being in a single integrated circuit.

33. The DC to DC switching circuit of claim 32 further comprising:

current sense circuits, the control circuits being responsive to the current sense circuits to tend to minimize a difference of current between the plurality of interleaved converter circuits.

34. The DC to DC switching circuit of claim 33 wherein the control circuits control the plurality of pulse width modulators.

35. The DC to DC switching circuit of claim 32 further comprising: an integrator having an output responsive to the integral of an error signal, the error signal being responsive to the voltage across the common load and a desired voltage.

36. The DC to DC switching circuit of claim 35, wherein the control circuits is also responsive to the output of integrator.

37. The DC to DC switching circuit of claim 35 wherein a time constant of the integrator is adjustable by the selection of at least one component external to the integrated circuit.

38. The DC to DC switching circuit of claim 35 further comprising a differentiator having an output responsive to a rate of change of the voltage across the common load, the

control circuits also being responsive to the output of differentiator.

39. The DC to DC switching circuit of claim 38 wherein a time constant of the differentiator is adjustable by the selection of at least one component external to the integrated circuit.

40. The DC to DC switching circuit of claim 32 wherein the control circuits are also responsive to rapid decreases in the voltage across the common load to turn on the plurality of converter circuits, independent of the phase of the plurality of pulse width modulators.

41. The DC to DC switching circuit of claim 32 wherein the control circuits are also responsive to rapid increases in the voltage across the common load to turn off the plurality of converter circuits, independent of the phase of the plurality of pulse width modulators.

42. The DC to DC switching circuit of claim 32, wherein the plurality of pulse width modulators consist of a pair of pulse width modulators.

43. The DC to DC switching circuit of claim 32 wherein the commanded output voltage is controllable through an input to the integrated circuit.

44. The DC to DC switching circuit of claim 32 wherein the feedback circuit is in the single integrated circuit.

45. A circuit in a DC to DC converter having a plurality of interleaved converter circuits operating into a common load, comprising:

a plurality of pulse width modulators each controlling power switching devices of one of the plurality of interleaved converter circuits;

control circuits for adjusting a nominal duty cycle of the plurality of interleaved converter circuits;

the plurality of pulse width modulators and the control circuits being in a single integrated circuit.

46. A DC to DC switching circuit for controlling power switching devices in a DC to DC converter having first and second interleaved converter circuits operating into a common load, comprising:

a first pulse width modulator controlling the power switching devices of the first converter circuit;

a second pulse width modulator controlling the power switching devices of the second converter circuit;

a feedback circuit responsive to the voltage across the common load;

control circuits for controlling the first and second pulse width modulators responsive to the feedback circuit;

the control circuits also being responsive current measurements through the first converter circuit and the second converter circuit for adjusting the relative duty cycle of the first and second converter circuits;

the first pulse width modulator, the second pulse width modulator, the feedback circuit and the control circuits being in a single integrated circuit.

CONCLUSION

In accordance with 37 C.F.R. § 1.173(b), Applicants respectfully submit herewith the proposed amendments for incorporation into the above-identified Reissue application. Reconsideration of pending claims 1-46 is respectfully requested.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 8, 2001

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: February 8, 2001.

Nancy Claeyssens — *Date* 2/8/01

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STATEMENT OF STATUS/SUPPORT FOR CLAIM CHANGES

BOX REISSUE
Assistant Commissioner for Patents
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Sir:

In accordance with 37 C.F.R. SECTION 1.173(c), claims 1-46 are now pending. Support in the disclosure of the patent for newly added claims 22-46 is listed below.

Claim Number	Support in Disclosure
Claim 22	Original claim 1; column 6, lines 21-25 of the printed patent
Claim 23	Original claim 1; column 1, lines 48-49 of the printed patent
Claim 24	Original claim 3

Claim 25	Original claim 4
Claim 26	Original claim 5
Claim 27	Original claim 6
Claim 28	Original claim 7
Claim 29	Original claim 8
Claim 30	Original claim 1; Figure 2a; Figure 2c
Claim 31	Original claim 1
Claim 32	Original claim 10; and column 1, lines 48-49 of the printed patent
Claim 33	Original claim 1; Column 3, lines 11-46 of the printed patent
Claim 34	Original claim 10
Claim 35	Original claim 13
Claim 36	Original claim 13
Claim 37	Original claim 14
Claim 38	Original claim 15
Claim 39	Original claim 16
Claim 40	Original claim 17
Claim 41	Original claim 18
Claim 42	Original claim 10; Figure 2a; and Figure 2c
Claim 43	Original claim 20
Claim 44	Original claim 21
Claim 45	Original claim 10; column 1, lines 48-49 of the printed patent
Claim 46	Original claim 10

In light of the foregoing, Applicant respectfully submits that no new substantive matter has been added and respectfully requests consideration of all pending claims.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 8, 2001

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Nancy Claeyssens — *Date* 2/8/01